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     (FILE 'HOME' ENTERED AT 15:33:16 ON 25 JUL 2003)
     FILE 'CA' ENTERED AT 15:33:32 ON 25 JUL 2003
L1  27122 S (SI OR SILICON OR POLYSI OR POLYSILICON)(4A)(WIRE OR CONDUCTOR OR
          ELECTRODE OR TRACE OR LINE OR TRACK)
L2   9436 S L1 AND(MEMS OR MICROELECTRON? OR INTEGRATED OR CIRCUIT OR IC OR
          SEMICONDUCT?)
L3     76 S L2 AND(FAIL? OR RELIAB? OR PROTECT? OR CORRO? OR
          LEAKAGE(3A)CURRENT)(6A)(DETECT? OR DETERMIN? OR DIAGNOS? OR ASSAY? OR
          ANALY? OR ASSES? OR MEASUR? OR MONITOR? OR TEST? OR ESTIMAT? OR
          EVALUAT? OR PROBE# OR PROBING OR EXAMIN? OR CHECK? OR PREDICT? OR
          QUANTITAT? OR QUANTIF? OR SIMULAT?)
     FILE 'INSPEC' ENTERED AT 15:45:03 ON 25 JUL 2003
L4    119 S L3
     FILE 'JICST-EPLUS' ENTERED AT 15:48:31 ON 25 JUL 2003
L5     10 S L3
     FILE 'CA, INSPEC, JICST-EPLUS' ENTERED AT 15:49:38 ON 25 JUL 2003
L6    181 DUP REM L3 L4 L5 (24 DUPLICATES REMOVED)
L7    147 S L6 NOT PY>1999

=> d l7 bib,ab 1-147

L7   ANSWER 5 OF 147  CA  COPYRIGHT 2003 ACS on STN
AN   131:162516  CA
TI   Passivation and corrosion of microelectrode arrays
AU   Schmitt, G.; Schultze, J.-W.; Fassbender, F.; Buss, G.; Luth, H.; Schoning,
     M. J.
CS   Laboratory for Corrosion Protection, Iserlohn University of Applied
     Science, Iserlohn, 58590, Germany
SO   Electrochimica Acta (1999), 44(21-22), 3865-3883
AB   A review with 64 refs. concerning passivation and corrosion of
     microelectrode arrays is presented.  Application of silicon based
     microsensors in electrolyte solns. is hampered by insufficient barrier
     properties and poor corrosion resistance of common passivation layers used
     to protect the underlying conducting tracks and microelectronic structures.
     Therefore, the protectivity of various types of compatible passivation
     layers (org. polyimide and photoresist films, inorg. mono, duplex and
     triplex layers based on PECVD silicon oxide and silicon nitride) was
     investigated and improved on microelectrode arrays exposed to 1 M NaCl (pH
     2 to 10) at 25°C.  Duplex SiO2/Si3N4 and oxide/nitride/oxide (ONO) triplex
     layers with optimized nitride PECVD process yielded the best barrier
     properties.  Burying the conducting tracks in the thermal silicon oxide
     layer improves the performance significantly.  Failures of the passivation
     layers, detected by leak current and layer resistance measurements with
     subsequent SEM investigation, result from cracking due to intrinsic and
     extrinsic (less important) mech. stress, film defects (pinholes, particle
     inclusions), from chem., physicochem. and electrochem. reactions (external,
     internal, sublayer corrosion) and from the combined action of mech. stress
     and chem. interaction (stress corrosion cracking).

L7   ANSWER 6 OF 147  CA  COPYRIGHT 2003 ACS on STN
AN   130:117769  CA
TI   "Copper chip" technology
AU   Edelstein, D. C.
CS   IBM T. J. Watson Research Center, Yorktown Heights, NY, 10598, USA
SO   Proceedings of SPIE-The International Society for Optical Engineering
     (1998), 3506(Microelectronic Device Technology II), 8-18
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AB A review with 17 refs. Recently, IBM announced the first silicon **integrated circuit** technol. that incorporates copper on-chip wiring. This technol., which combines industry-leading CMOS ULSI devices with 6 levels of hierarchically-scaled Cu metalization, has reached the point of manufg., after passing the qualification **tests** required to prove feasibility, yield, **reliability**, and manuf.. The discussion of the change from Al to Cu interconnects for ULSI encompasses a wide variety of issues. This paper attempts to address these by way of example, from the broad range of detailed studies that have been performed in the course of developing these so-called "copper chips". Motivational issues are covered by comparative modeling of performance aspects and cost. The technol. parameters and features are shown, as well as data relating to the process integration, elec. yield and parametric behavior, early manufg. data, high-frequency modeling and measurements, noise and clock skew. The viability of this technol. is indicated by results from reliability stressing, as well as the first successful demonstrations of fully functional SRAM, DRAM, and microprocessor chips with Cu wiring. The advantages of **integrated** Cu wiring may be applied even more broadly in the future. An example shown here is the achievement of very high-quality **integrated** inductors; these may help prospects for complete integration of RF and wireless communications chips onto silicon.

L7 ANSWER 9 OF 147 CA COPYRIGHT 2003 ACS on STN
AN 128:288838 CA
TI Post metal etch polymer removal process. The elimination of an intermediate rinse step
AU Graham, Sandra W.
CS SEMITOOL, Inc., Kalispell, MT, 59901, USA
SO Proceedings - Electrochemical Society (1998), 97-35(Cleaning Technology in Semiconductor Device Manufacturing), 587-593
AB To achieve the necessary device performance, complete removal of residual polymer created during the plasma etch and photoresist strip process is crit. In addn., it is essential that the residue removal process not compromise the integrity of the metal lines. This work evaluates the impact of various post metal etch polymer removal processes on corrosion and/or attack of Al-Cu-**Si** metal **lines**. Two of the five process sequences **evaluated** resulted in no attack or **corrosion** of the metal lines.

L7 ANSWER 11 OF 147 CA COPYRIGHT 2003 ACS on STN
AN 126:193645 CA
TI Various contrasts identifiable from the backside of a chip by 1.3 μm laser beam scanning and current change imaging
AU Nikawa, K.; Inoue, S.
CS NEC Corporation, Kawasaki, Japan
SO ISTFA '96, Proceedings of the International Symposium for Testing and Failure Analysis, 22nd, Los Angeles, Nov. 18-22, 1996 (1996), 387-392 Publisher: ASM International, Materials Park, Ohio.
AB We can identify various contrasts by scanning an 1.3 μm laser beam from the backside of a chip and displaying current changes as brightness changes on a CRT, because the 1.3 μm laser beam generates no OBIC signal and can penetrate P- Si substrate with little intensity degrdn. The contrasts we have confirmed up to now are:. (1) Current pass contrast at Al lines caused by OBIRCH, (2) Defect contrast at Al interconnects caused by OBIRCH, (3) Current pass contrast at a poly **Si lines** caused by OBIRCH, (4) Parasitic MIM (metal-insulator-metal) contrast caused by temp. dependence of MIM current, (5) Schottky-barrier contrast caused by internal photoemission.

L7 ***ANSWER 12 OF 147 CA*** COPYRIGHT 2003 ACS on STN
AN 125:313513 CA
TI A hermetic glass-silicon micropackage with high-density on-chip feedthroughs for sensors and actuators
AU Ziaie, Babak; Von Arx, Jeffrey A.; Dokmeci, Mehmet R.; Najafi, Khalil
CS Center Integrated Sensors and Circuits, University Michigan, Ann Arbor, MI, 48109-2122, USA
SO Journal of Microelectromechanical Systems (1996), 5(3), 166-179
AB This paper describes the development of a hermetic micropackage with high-d. on-chip feedthroughs for sensor and actuator applications. The packaging technique uses low-temp. (320°) electrostatic bonding of a custom-made glass capsule (Corning #7740, 2×2×8 mm3) to fine grain polysilicon to form a hermetically sealed cavity. High-d. on-chip multiple polysilicon feedthroughs (200 per mm) were used for connecting external sensors and actuators to the electronic circuitry inside the package. A high degree of planarity over feedthrough areas was obtained by using grid-shaped **polysilicon** feedthrough **lines** that are covered with phosphosilicate glass (PSG), which is subsequently reflown at 1100° in steam for 2 h. Saline and DI H2O soak tests at elevated temps. (85 and 95°) were performed to **det**. the **reliability** of the package. Preliminary results showed a mean time to failure (MTTF) of 284 days and 118 days at 85 and 95°, resp., in DI H2O. An Arrhenius diffusion model for moisture penetration yields an expected lifetime of 116 yr at body temp. (37°) for these packages. In vivo tests in guinea pigs and rats for periods ranging from one to two months showed no sign of infection, inflammation, or tissue abnormality around the implanted package. [181].

L7 ANSWER 18 OF 147 CA COPYRIGHT 2003 ACS on STN
AN 124:19188 CA
TI The detrimental effect of a passivation on the electromigration lifetime of narrow Al-**Si**-Cu **lines**
AU Witvrouw, A., Ph.; Deweerdt, B.; Maex, K.
CS IMEC, Louvain, 3001, Belg.
SO Materials Research Society Symposium Proceedings (1995), 391(Materials Reliability in Microelectronics V), 447-52
AB 2 Mm long, 0.8 μm wide and 0.8 μm thick Al-**Si**-Cu **lines**, passivated with a 1.14 μm thick PETEOS SiO2 were found to have a lower electromigration lifetime compared to identical unpassivated lines. The high tensile stress in the passivated lines is assumed to accelerate electromigration failure. This is confirmed by the very low activation energy for electromigration failure in the passivated lines and by the multiple events of recovery during and after electromigration **testing**, suggesting **failure** sites are slit voids.

L7 ***ANSWER 21 OF 147*** CA COPYRIGHT 2003 ACS on STN
AN 122:175490 CA
TI Detection and prevention of polysilicon filaments along field oxide isolation edges
AU Gabriel, Calvin; Johnson, Eric; Dimitrelis, Dimitrios; Nowak, Edward
CS VLSI Technology, Inc., San Jose, CA, 95131, USA
SO Proceedings - Electrochemical Society (1994), 94-20(Proceedings of the Tenth Symposium on Plasma Processing, 1994), 281-90
AB When **current leakage** was **detected** between tightly spaced polycide gates, SEM micrographs revealed polysilicon filaments caused by residual polysilicon filling a notch at the field oxide edge. A test structure with interdigitated **polysilicon lines** having variable spacing over severe LOCOS topog. was designed to allow rapid detection of such polysilicon filaments. The test structure was used to optimize polysilicon overetch time. The

min. overetch time required to prevent filament formation depends on the spacing between lines and on LOCOS isolation processing parameters.

L7 ANSWER 23 OF 147 CA COPYRIGHT 2003 ACS on STN
AN 121:242802 CA
TI Evaluation of non-hermetic coatings for MCM applications through HAST, 85/85 and PCT
AU Murphy, Cynthia F.; Kodnani, Ramesh; Peterson, David W.
CS Microelectron. Comput. Technol. Corp., Austin, TX, 78727, USA
SO Proceedings of SPIE-The International Society for Optical Engineering (1994), 2256(Multichip Modules), 338-43
AB The goal of the Reliability without Hermeticity (RwoH) Project is to find non-hermetic coatings for use on MCMs. As a means of down-selecting coating materials, Sandia ATC01 test chips in 40 pin DIPs were coated with non-hermetic, polymer materials, including silicone gel, filled epoxy, and polyimide. After preconditioning through temp. cycling and salt atm., the parts were subjected to one of three different temp., humidity, and bias conditions: HAST (140°C, 85% RH, +40V), 85/85 (85°C, 85% RH, +40V), or PCT (121°C, 99.6% RH). No universal relationship between lifetime in HAST and 85/85 testing was obsd.--the effects appear to be material dependent. Elec. **test** data suggest that **failures** on coated parts (with std. SiN chip passivation) do not occur on die circuitry (triple tracks) and instead occur on bond-wires and bond-pads.

L7 ANSWER 38 OF 147 CA COPYRIGHT 2003 ACS on STN
AN 105:33713 CA
TI **Reliability evaluation** of plastic packaged devices for long life applications by the temperature-humidity-bias test
AU Brambilla, P.; Canali, C.; Fantini, F.; Magistrali, F.; Mattana, G.
CS Reliab. Qual. Dep., Telettra S.p.A., Vimercate, 20059, Italy
SO Microelectronics and Reliability (1986), 26(2), 365-384
AB The reliability of transistors and bipolar and complementary MOS (CMOS) **integrated circuits** encapsulated in different types of plastic packages was investigated by using the 85°/85% relative-humidity (R.H.) test with applied bias and the results compared with a long term operating life test. Particular attention was devoted to pointing out the effect of technol., process control, and working conditions on device reliability and failure mechanisms. In micropackaged transistors the importance of surface passivation in protecting the devices against Au corrosion was focused, while the need of good process control was confirmed by the results of the test on micropackaged linear **integrated circuits**. In dual-in-**line** CMOS **integrated circuits**, **Si** nitride and polyimide give, in general, superior protection, but good results were obtained also with normal P-glass passivation when a clever arrangement of layout design rules was adopted. A significant improvement was obtained in the reliability of plastic packaged devices, with the best figures showing no failures after 15,000 h at 85°/85% R.H. test with bias.

L7 ANSWER 39 OF 147 CA COPYRIGHT 2003 ACS on STN
AN 104:197896 CA
TI **Corrosion failure** modes in TAB200 **test** vehicle
AU Padmanabhan, Ramaswamy
CS Motorola, Inc., Phoenix, AZ, 85008, USA
SO IEEE Transactions on Components, Hybrids, and Manufacturing Technology (1985), CHMT-8(4), 435-9
AB Temp.-humidity bias tests were carried out for tape automated bonded (TAB) samples, consisting of Au/Cu/Cr metal bump structures and Al/**Si** interconnecting metalization **tracks**, passivated with P-doped glass. Three

predominant failure modes were identified: (1) type A failure: corrosion of pos. and neg. metalization tracks; (2) type B failure: corrosion at the bond pad-bump interfaces; and (3) type C failure: debonding of the Cu/Sn inner leads from the bumps. While type C failure was mainly due to improper bonding parameters and thus not directly related to the corrosion process, the other 2 types were caused by specific ionic impurities. Adhesion between the various metal-passivation interfaces and the quality of the passivation both had a major effect on the corrosion characteristics.

L7 ANSWER 52 OF 147 CA COPYRIGHT 2003 ACS on STN
AN 95:142513 CA
TI Electromigration resistance of fine-line aluminum for VLSI applications
AU Vaidya, S.; Fraser, D. B.; Sinha, A. K.
CS Bell Lab., Murray Hill, NJ, 07974, USA
SO Annual Proceedings - Reliability Physics [Symposium] (1980), 18th, 165-70
AB The electromigration lifetimes were detd. for an as-yet unexplored combination of long lines (≤3 cm) and narrow linewidths (≥1 μm) of evapd. and magnetron sputter-source deposited Al-Cu-Si films. The lifetimes for the sputtered films are significantly smaller than those for electron-beam evapd. films. The latter displayed an unusually large improvement in the lifetime for finer linewidths (1.5 and 1 μm). **Failure** modes were **analyzed** and correlations made with a new microstructural parameter incorporating the film grain-size, its σ and the degree of preferred orientation.

L7 ANSWER 80 OF 147 INSPEC (C) 2003 IEE on STN
AN 1996:5366690 INSPEC DN B9610-2550-008
TI Diagnostic and monitoring tools of large scale **Si**-manufacturing: **trace**-analytical tools and techniques in Si-wafer manufacturing.
AU Fabry, L.; Koster, L.; Pahlke, S.; Kotz, L.; Hage, J. (Wacker Siltronic GmbH, Burghausen, Germany)
SO IEEE Transactions on Semiconductor Manufacturing (Aug. 1996) vol.9, no.3, p.428-36. 87 refs.
AB In order to facilitate fast corrective actions, all process media, crucial process steps and intermediate product stages of wafering must be monitored by suitable **analytical** tools. The **analyzes** have to provide **reliable**, relevant and real-time results at justifiable economy. Preferably, they should be serviceable in on-line configuration under strict SPC conditions. The following chapters outline the performance of the few analytical techniques, that optimally satisfy these requirements.

L7 ANSWER 87 OF 147 INSPEC (C) 2003 IEE on STN
AN 1995:5039161 INSPEC DN B9510-2560R-022
TI Analytical predictions of thermal stress in MOSFETs.
AU O'Connor, J. (Aerosp. Corp., El Segundo, CA, USA)
SO 1995 IEEE Aerospace Applications Conference. Proceedings (Cat. No.95TH8043) New York, NY, USA: IEEE, 1995. p.131-43 vol.2 of 2 vol. (xiv+414+340) pp. 7 refs.
AB The present work contains a discussion of finite-element stress analyses of NMOS devices performed in support of an experimental study of VLSI device reliability. The purpose of the experimental study is to examine the effects of varying line geometry on device performance parameters such as threshold voltage, source-drain breakdown, and substrate current. The purpose of the analytical work is to characterize the residual thermal stresses in the devices for correlation with experimental **reliability measurements**. The devices consist of a silicon substrate underlying a thermally grown gate oxide, with a **polysilicon line** structure encapsulated by low-temperature oxide. Plane stress analyses of devices with three line

thicknesses were performed. An analogous three-dimensional analysis was performed of one of the plane stress cases in order to show the effect of the plane stress assumption on calculated results. A three-dimensional analysis of the encapsulated structure also was performed. Results indicate that residual stresses in the substrate and gate oxide due to thermal processing are probably high enough to cause degradation or failure of the devices.

L7 ANSWER 91 OF 147 INSPEC (C) 2003 IEE on STN
AN 1995:4907078 INSPEC DN B9505-2550F-004
TI On the ASTM electromigration test structure applied to Al-1% **Si**/TiN/Ti bamboo metal **lines**.
AU De Munari, I. (Dipartimento de Ingegneria dell'Inf., Parma Univ., Italy); Vanzi, M.; Scorzoni, A.; Fantini, F.
SO Quality and Reliability Engineering International (Jan.-Feb. 1995) vol.11, no.1, p.33-9. 15 refs.
AB The applicability of NIST-ASTM electromigration test patterns when used to test 'bamboo' metal lines is discussed. Wafer level tests on passivated add non-passivated samples employing the Al-1%Si/TiN/Ti metallization scheme were performed. Straight metal lines of 1000 mu m long and 0.9 mu m or 1.4 mu m wide were tested at two different current densities, j=3 MA/cm2 and j=45 MA/cm2, at constant stress temperature (T=230 degrees C). The failures mainly occurred in the end-segment areas and hindered the evaluation of the electromigration resistance of the 'bamboo' test lines. In order to avoid this problems, completely different test patterns based on different approaches must be designed.

L7 ANSWER 125 OF 147 INSPEC (C) 2003 IEE on STN
AN 1984:2160532 INSPEC DN B84000671
TI **Failure analysis** of double polysilicon thick interlevel oxide **failures** (in RAMs).
AU Renaud, D.P.; Holden, D.M. (IBM General Technol. Div., Essex Junction, VT, USA)
SO Proceedings of ISTFA 1982 International Symposium for Testing and Failure Analysis Torrance, CA, USA: ISTFA, 1982. p.104-10 of xi+363 pp. 4 refs.
AB **Failure analysis** can help improve the **reliability** of **semiconductors**. This paper demonstrates how **failure analysis** assisted in identifying the process area responsible for reliability failures as well as demonstrating that failures were defect-related and not a fundamental problem with the structure. Most failures were found to occur at the polysilicon I thick oxide sidewall region. Many failures were related to foreign material that was introduced prior to oxide growth. It was observed that 10 of the 12 failures occurred at the polysilicon sidewall and all 10 failures were located on the same side of the **polysilicon conductors** when oriented to the wafer pattern. The accelerated life stressing was performed using a test site chip specifically designed to simulate the gate areas used on a random access memory (RAM). The test site stress conditions were designed to produce failures in the early hours of stress.

L7 ANSWER 130 OF 147 INSPEC (C) 2003 IEE on STN
AN 1981:1762288 INSPEC DN A81100675; B81050894
TI Thin film metallization studies and device lifetime prediction using Al-**Si** and Al-Cu-**Si conductor** test bars.
AU Danso, K.A.; Tullos, L. (MOSTEK Corp., Carrollton, TX, USA)
SO Microelectronics and Reliability (1981) vol.21, no.4, p.513-27. 26 refs.
AB In this work, Al-Si and Al-Cu-Si metallizations were fabricated to run over a topology similar to a typical double-poly N-channel MOS **IC**, with numerous steps and contacts. It was found that the contacts and steps were more

susceptible to metallization failures. However with process variation to improve step coverage, and also with Cu doping, an improvement in lifetime of 20 and 50 respectively could be obtained. An electromigration current density relationship of J-1.70 was obtained, indicating that an error of about 56 times could be made, thereby underestimating device lifetime prediction if a value of J-2 was assumed as is normally done.

L7 ANSWER 141 OF 147 INSPEC (C) 2003 IEE on STN
AN 1969:54652 INSPEC DN B69017164
TI Failure mechanisms in large-scale **integrated circuits**.
AU Schnable, G.L.; Keen, R.S., Jr.
SO IEEE Transactions on Electron Devices (April 1969) vol.ED-16, no.4, p.322-32. 41 refs.
AB A study was made of the factors affecting the reliability of large-scale **integrated** (LSI) **circuits**. Particular attention was given to the effect on array reliability of the additional processing steps required to obtain multilevel metalization. The additional significant steps are low temperature deposition of a second dielectric layer on metalized LSI wafers, etching of vias through the second dielectric, and second level metalization. Consideration was also given to the effect of other trends in LSI, such as the use of smaller geometry and closer spacings. Possible new failure modes in multilevel arrays are shorts or increased leakage through or along deposited second layer dielectrics, opens or increased series resistance in **conductors**, and **silicon** surface effects. A review of literature on LSI was supplemented by results of a number of concurrent LSI programs and experimental studies. Test vehicles were designed to provide fundamental information about each of the categories of **failure**. Data obtained using these **test** vehicles to evaluate the multilevel metalized array structures are presented. A discussion concerning the merits and limitations of the specially-designed test vehicles for process development, process control, and **reliability tests** is given. It is concluded that with the proper in-process controls, tests and screens, LSI arrays will be substantially more reliable per function accomplished than are conventional **integrated circuits**.

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STN INTERNATIONAL LOGOFF AT 15:51:32 ON 25 JUL 2003